

## NOTES (UNLESS OTHERWISE SPECIFIED):

- THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).
- THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
- BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98  
T<sub>g</sub> - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.  
T<sub>d</sub> - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.  
E<sub>r</sub> - MUST BE FROM 4.2 TO 4.4
- COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
- CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B'
- MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .0045"/.005"
- PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):  
.05080-.232 MICRON (2-8 MICROINCH) OF GOLD OVER  
2.540-6.350 MICRON (100-250 MICROINCH) OF NICKEL.
- ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.
- SOLDERMASK - GREEN COLOR BOTH SIDES.  
MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM FREESCALE.
- SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.
- ELECTRICAL TEST - 100% IPCD356.
- PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.
- DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS.  
UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE.
- TEARDROPS MAYBE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.
- 2 SOLDER SAMPLES TO BE PROVIDED.
- BASIC GRID INCREMENT AT 1:1 IS .0001.
- SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.  
- MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0
- THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (Pb)
- THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)
- ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP.  
ALL HOLE LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM.
- FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS.  
THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.
- INTENTIONAL SHORTS AT:  
SH3 P3V3 & N20114060  
SH4 SPI\_CLK & N20113927:  
SH7 SPI\_SS & N20113921  
SH8 KW40\_SWD\_CLK & N20113933  
SH9 SWD\_DIO\_TGTMCU & N20113935  
SH10 BUZZER & N20092069  
SH11 INT1\_COMBO & N20092076  
SH12 SW3 & N20092083  
SH13 SW4 & N20092090  
SH14 ELEC\_IN2 & N20092097  
SH15 ELEC\_IN1 & N20092104  
SH20 PTC4 & N20755276  
SH21 SWD\_DIO\_TGTMCU & N20755278  
SH22 BUZZER & N20755274  
SH23 PTC5 & N20755280  
SH24 PTC4 & N20064946  
SH25 PTB17 & N20184312  
SH26 ADC0\_SE0/BATTERY\_MONITORING & N20065047  
SH27 ADC0\_SE1/POT & N20065043  
SH28 PTB16 & N20184318  
SH29 CMT & N20184324  
SH30 PTC5 & N20184330  
SH31 COM & N20065031  
SH33 PTB18 & N20065027  
SH500 V\_TGTMCU & P3V3  
SH501 P3V3\_SDA & SDA\_VOUT33  
SH503 P3V3\_LED & P3V3  
J12 SWD\_CLK\_TGTMCU & KW40\_SWD\_CLK  
J13 SWD\_DIO\_TGTMCU\_BUF & SWD\_DIO\_TGTMCU  
J14 SWD\_CLK\_TGTMCU\_BUF & SWD\_CLK\_TGTMCU  
J25 SDA\_RST\_TGTMCU\_J\_B & SDA\_RST\_TGTMCU\_B

8 ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.

9. SOLDERMASK - GREEN COLOR BOTH SIDES.  
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10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.

11. ELECTRICAL TEST - 100% IPCD356.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

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UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE.

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16. BASIC GRID INCREMENT AT 1:1 IS .0001.

17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.  
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18. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (Pb)

19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

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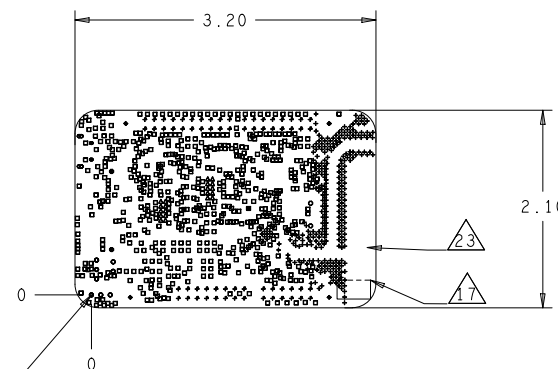
21. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS.  
THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.

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J13 SWD\_DIO\_TGTMCU\_BUF & SWD\_DIO\_TGTMCU  
J14 SWD\_CLK\_TGTMCU\_BUF & SWD\_CLK\_TGTMCU  
J25 SDA\_RST\_TGTMCU\_J\_B & SDA\_RST\_TGTMCU\_B

23. INTENTIONAL SHORT ON TOP LAYER BETWEEN RF\_ANT AND GND

24. OVERALL PCB DIELECTRIC THICKNESS ARE TARGETED (A & C) 10 MILS +/-10% AND (B) 38 MILS +/-10%  
AS SHOWN IN DETAIL 'A'. ADJUSTMENT IN SUBSTRATE B IS ALLOWED TO MEET OVERALL HEIGHT REQUIREMENT.



0.062" THICK +/- 10%

DETAIL B  
IMPEDANCE REQUIREMENTS  
IMPEDANCE TOLERANCE IS 10%  
PRIMARY DATUM  
GRID ORIGIN

Layers	Single Ended		Differential		Differential		
	Trace Width (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing "Airgap" (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing "Airgap" (Mils)
LI_PS	18.00	50	11.5	6.00	90	8.50	6.00

24 0.062" +/-10%

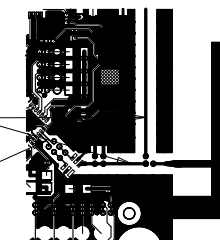


LAYER 1 TOP SIDE 1 oz.  
LAYER 2 GROUND PLANE 1 oz.  
LAYER 3 INTERNAL 1 1 oz.  
LAYER 4 BOTTOM SIDE 1 oz.

DETAIL A  
LAYER STACKUP  
SCALE: NONE

FINISHED Cu WEIGHT

50 OHMS SINGLE ENDED  
TRACE: 18 MILS +/-10%  
100 OHMS DIFF PAIR  
TRACE: 8.5 MILS WIDTH  
SPACING: 6 MILS



DRILL CHART: TOP to BOTTOM ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
+	8.0	+0.0/-8.0	PLATED	283
■	10.0	+0.0/-10.0	PLATED	564
•	12.0	+0.0/-12.0	PLATED	2
•	12.0	+2.0/-2.0	PLATED	2
▲	28.0	+2.0/-2.0	PLATED	20
■	35.0	+2.0/-2.0	PLATED	59
•	40.0	+3.0/-3.0	PLATED	8
+	42.0	+3.0/-3.0	PLATED	64
■	63.0	+3.0/-3.0	PLATED	1
•	73.0	+3.0/-3.0	PLATED	2
•	125.0	+3.0/-3.0	NON-PLATED	4
•	34.0x26.0	+2.0/-2.0	PLATED	2
•	60.0x33.0	+2.0/-2.0	PLATED	2

DETAIL B

PART NO. 170-28379		FREESCALE	
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO FREESCALE AND SHALL NOT BE USED FOR ENGINEERING DESIGN OR IN PART WITHOUT THE CONSENT OF FREESCALE.		6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA	
TITLE: PRINTED WIRING BOARD FRDM-KW40Z		REV C2	
SCALE 1/1		DO NOT SCALE DRAWING	
SHEET 1 OF 1			